OIPE JC130
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2631

PATENT
450117-03309

#4
10-18-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Jens WILDHAGEN
Serial No.	:	09/863,487
Filed	:	May 23, 2001
For	:	A DIGITAL FILTER FOR IQ-GENERATION, NOISE SHAPING AND NEIGHBOUR CHANNEL SUPPRESSION
Art Unit	:	2631

745 Fifth Avenue
New York, New York 10151
Tel. (212) 588-0800

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Gordon Kessler, Reg. No. 38,511
Name of Applicant, Assignee or Registered Representative

Gordon Kessler
Signature

September 14, 2001
Date of Signature

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CLAIM OF PRIORITY

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In support of the claim of priority under 35. U.S.C. § 119 asserted in the Declaration accompanying the above-entitled application, as filed, please find enclosed herewith a certified copy of European Application No. 00 111 193.9, filed in Europe on 24 May 2000 forming the basis for such claim.

PATENT
450117-03309

Acknowledgment of the claim of priority and of the receipt of said certified copy(s) is requested.

Respectfully submitted,

FROMMER LAWRENCE & HAUG LLP
Attorneys for Applicant

By: Gordon Kessler

Gordon Kessler
Reg. No. 38,511
Tel. (212) 588-0800

Enclosure

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Bescheinigung | Certificate | Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

00111193.9

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

Anmeldung Nr.:
Application no.: 00111193.9
Demande n°:

Anmeldetag:
Date of filing: 24/05/00
Date de dépôt:

Anmelder:
Applicant(s):
Demandeur(s):
Sony International (Europe) GmbH
10785 Berlin
GERMANY

Bezeichnung der Erfindung:
Title of the invention:
Titre de l'invention:
A digital filter for IQ-Generation, noise shaping and neighbour channel suppression

In Anspruch genommene Prioriät(en) / Priority(ies) claimed / Priorité(s) revendiquée(s)

Staat: State: Pays:	Tag: Date: Date:	Aktenzeichen: File no. Numéro de dépôt:

Internationale Patentklassifikation:
International Patent classification:
Classification internationale des brevets:
H03H17/02

Am Anmeldetag benannte Vertragstaaten:
Contracting states designated at date of filing: AT/BE/CH/CY/DE/DK/ES/FI/FR/GB/GR/IE/IT/LI/LU/MC/NL/PT/SE/TR
Etats contractants désignés lors du depôt:

Bemerkungen:
Remarks:
Remarques:

MÜLLER & HOFFMANN PATENTANWÄLTE

European Patent Attorneys - European Trademark Attorneys

Innere Wiener Strasse 17
D - 81667 München

Attorney's File: 50679 Gö/sat 24.05.2000
Client's Ref.: S97P5091EP00/PAE97-046STC

Sony International (Europe) GmbH
Kemperplatz 1
10785 Berlin

A Digital Filter For IQ-Generation, Noise Shaping and Neighbour Channel Suppression

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Description

The present invention relates to the digital generation of a complex baseband signal and in particular to an efficient realization of a polyphase-filter which can be used therefore and also for other purposes.

The German Patent Application DE 43 32 735 A1 "Verfahren zur digitalen Erzeugung eines komplexen Basisbandsignals" describes an algorithm for the generation of a complex baseband signal which makes use of a polyphase-filter. This Patent Application also describes that the branch filters of the polyphase-filter should be realized as allpass filters.

The paper "Entwurf und Realisierung diskreter Filterbänke", published by Shaker, ISBN 3-8265-0366-X, from Torsten Leickel explains how to design such polyphase-filters with allpass branch filters.

In this case, the input signal of the polyphase-filter is multiplexed into N different allpass filters. Therefore, N allpass filters have to be realized with N being the decimation factor of the polyphase filter. This design leads to high realization costs for the polyphase-filter. Also, only a restricted amount of IF-frequencies can be realized with this structure, since the IF-frequencies can only be chosen to $F_{IF}=m \cdot F+L \cdot F/N$ with F being the sampling rate of the filter input signal, L being a natural constant between $\frac{-N-1}{2} \dots \frac{N-1}{2}$ and m being a natural constant.

Further, EP 0 597 255 A1 "Empfänger für ein digitales Rundfunksignal mit digitaler Signalverarbeitung" discloses an efficient realization of an algorithm for the generation of a complex baseband signal. To optimize the realization of the digital signal processing a switchable allpass filter is used. However, this realization has the disadvantage that no digital neighbour channel suppression/noise shaping can be realized and the IF-frequency can only be chosen to $F_{IF}=m \cdot F \pm F/4$ with F being the IQ-filter input sampling rate and m being a natural constant.

However, all of the above IQ-generators are quite restricted in respect to the used Intermediate Frequency (IF) and therewith in respect to possible sampling frequencies of the A/D converter converting the IF signal into a signal suitable

for a following digital baseband processing since the output frequency of the generation is fixed according to certain standards and the input frequency of the IQ generation (i. e. the IF frequency) strongly depends on the used IQ-filter and the needed output frequency.

Therefore, it is an object underlying the present invention to provide a polyphase-filter which can be used for the IQ-generation and an IQ-generator providing an increased number of possible Intermediate Frequencies, i. e. more flexibility in the choosing of the sampling frequency of the A/D converter preceding the IQ generation.

A polyphase filter consisting of N branch allpass filters of order $x \cdot N$ to filter an input signal t(k) according to the present invention is defined in independent claim 1. Preferred embodiments thereof are defined in dependent claims 2 to 7.

The polyphase filter according to the present invention has low realization costs, since only a very small amount of adders and multipliers are required. In a preferred embodiment every needed multiplier is realized by at least one shift register, at least one adder and at least on subtracter, so that the realization costs are additionally decreased.

Furthermore, the using of a multiplexing technology allows a very easy adaptation to a different "number" of branch filters and therewith to a different IF frequency.

An IQ-generator according to the present invention is defined in independent claim 8. Preferred embodiments thereof are defined in dependent claims 9 and 10.

The IQ generator according to the present invention allows a very easy doubling of possible Intermediate Frequencies for a given polyphase filter consisting of N branch allpass filters of order $x \cdot N$ used therein, since signal symmetrics are used in an efficient way.

Preferably, the IQ-generator according to the present invention comprises a polyphase filter according to the present invention which allows to replace the

expensive analog filters in front of the A/D-converter by weak, cheap filters, since the polyphase filter according to the present invention allows a noise shaping and neighbour channel suppression in an easy way so that the effective resolution of the A/D-converter will be increased.

The present invention which uses and modifies the structure of conventional allpass filters first order to realize a polyphase filter of order $x \cdot N$ will be better understood from the following detailed description of exemplary embodiments thereof taken in conjunction with the accompanying drawings, wherein

Fig. 1	shows a block diagram of the N time multiplexed branch allpass filters of the polyphase filter according to a first preferred embodiment of the present invention;
Figs. 2a and 2b	show how the design of the polyphase branch allpass filters of order N according to the first preferred embodiment of the present invention was achieved;
Fig. 3	shows polyphase branch allpass filters according to a second preferred embodiment of the present invention;
Fig. 4	shows how the design of the polyphase filter according to the second preferred embodiment of the present invention was achieved;
Fig. 5	shows a block diagram of the system environment of an IQ-filter;
Fig. 6	shows a block diagram of a digital IQ-filter;
Fig. 7	shows a block diagram of a digital IQ-filter in case of quarter period sampling;
Fig. 8	shows a block diagram of the digital IQ-filter according to a preferred embodiment of the present invention; and
Fig. 9	shows an efficient realization of the IQ-filter shown in Fig. 8.

In the following the first preferred embodiment of a polyphase filter according to the present invention will be explained in connection with Figs. 1 and 2.

Fig. 2a shows a state of the art allpass filter of order 1 which comprises two delay elements 101 and 102, one adder 103, one subtracter 104 and one multiplier 105. Both delay elements have a delay T and the multiplier has a multiplication factor α. The structure of the state of the art allpass filter of order 1

shown in Fig. 2a is such that an input signal t(k) is fed to an input delay element 101 and as minuent to the subtracter 104. The delayed input signal output by the delay element 101 is input as a first summand to the adder 103 that produces and outputs the output signal u(k) of the allpass filter. The output signal u(k) is fed to an output delay element 102 which outputs the subtrahend for the subtracter 104. The difference calculated by the subtracter 104 gets multiplied with the multiplication factor α by the multiplier 105 and the resulting product is supplied as second summand to the adder 103 which adds its first and second summands to produce its output signal.

Equation (1) describes the transfer function of a polyphase lowpass filter with N filter branches, e. g. shown in "Multirate digital signal processing: multirate systems, filterbanks, wavelets", by N. J. Fliege, ISBN 0-471-93976-5:

$$H_{lp}(z) = \sum_{r=0}^{N-1} z^{-r} H_r(z^N) \qquad (1)$$

with $z = e^{j\Omega}$

$$\Omega = 2\pi \frac{f}{f_s},$$

$$j = \sqrt{-1}$$

As described in the DE 43 32 735 A1 or the publication "A new design method for polyphase filters using allpass sections" by W. Drews & L. Garrsi, IEEE Transactions on Circuits and Systems, Vol. CAS33, No. 3, March 1986, the branch filters can be chosen as state of the art allpass filters. The transfer function of such an allpass filter of order 1 which is shown in Fig. 2a is given in equation (2).

$$H_{ap,\,1^{st}\,order}(z) = \frac{U(z)}{T(z)} = \frac{\alpha + z^{-1}}{1 + \alpha z^{-1}} = \frac{\alpha z + 1}{z + \alpha} \qquad (2)$$

With equations (1) and (2) follows the transfer function of a branch allpass filter of the polyphase filter with one coefficient as shown in equation (3):

$$H_r(z^N) = \frac{\beta_r z^N + 1}{z^N + \beta_r} \qquad (3)$$

Therefore, with equations (1) and (3) follows the transfer function of the polyphase lowpass filter as shown in equation (4):

$$H_{lp}(z) = \sum_{r=0}^{N-1} z^{-r} \frac{\beta_r z^N + 1}{z^N + \beta_r} \qquad (4)$$

To realize a polyphase lowpass filter with a transfer function as shown in equation (4) according to the present invention, the N branch allpass filters are realized time-multiplexed with a sampling rate of $f_S' = f_S / N$ with f_S being the sampling rate of the polyphase filter input signal t(k).

Fig. 2b shows the structure of these N time-multiplexed allpass filters of order N with a sampling rate of $f_S' = f_S / N$ which is only different to the allpass filter first order shown in Fig. 2a in that the delay elements now have order N and the sampling rate is decreased, since the sampling rate decimation by N at the output of the polyphase filter is shifted to the input of the branch filter.

The transfer function of each of the N time-multiplexed allpass filters is calculated as follows:

With $f_s' = \frac{f_s}{N}$ and $\Omega' = 2\pi \frac{f}{f_s'}$, follows equation (5):

$$\Omega' = 2\pi \frac{Nf}{f_s} = N\Omega. \qquad (5)$$

With $z' = e^{j\Omega'}$ and equation (5) follows equation (6):

$$z' = e^{j\Omega'} = e^{jN\Omega} = z^N \qquad (6)$$

With equation (6) follows for the transfer function (7) of the N time-multiplexed allpass filters N^{th} order in consideration of the delay caused by the time-multiplex:

$$H_{ap',\,1^{st}\,order}(z^N) = \frac{U(z^N)}{T(z^N)} = z^{-r} \frac{\alpha z^N + 1}{z^N + \alpha} \qquad (7)$$

with r = 0, 1, ..N - 1.

In the preferred embodiment, aditionally the coefficient α of the N time-multiplex allpass filters is replaced by N time-multiplexed coefficients $\alpha_0, ..\alpha_{N-1}$ as

shown in equation (8):

$$\alpha(k) = \alpha_{(k \bmod N)} \tag{8}$$

The N time-multiplexed allpass filters of order N with the sampling rate $f_S' = f_S \cdot N$ included in the polyphase filter according to the first preferred embodiment of the present invention have now the following transfer functions as shown in equation (9):

$$H_{ap_r', 1^{st} order}(z^N) = \frac{U(z^N)}{T(z^N)} = z^{-r}\frac{\alpha_r z^N + 1}{z^N + \alpha_r} \tag{9}$$

with r = 0, 1, ..N - 1.

The block diagram of this polyphase branch filter realization according to the first preferred embodiment of the present invention is shown in Fig. 1 which basically shows the same structure as Fig. 2b, but the multiplier now comprises N time-multiplexed coefficients as described above.

Therefore, the polyphase filter according to the first preferred embodiment of the present invention comprises: a first delay element 1 with a delay N that receives the input signal t(k); a first adder 3 that receives the output signal of said first delay element 1 at a first input for the first summand; a second delay element 2 with a delay N that receives the sum produced by said first adder 3; a first subtracter 4 that receives the input signal t(k) at a first input for the minuend and the output signal of the second delay element 2 at a second input for the subtrahend; and a first multiplier 5 that receives the calculated difference of the first subtracter 4, multiplies it respectively with a predetermined multiplication coefficient α(k) and outputs the calculated product to a second input of the first adder 3 that receives the second summand, wherein in the sum produced by said first adder 3 builds the output signal u(k) of the filter.

The allpass branch filters of the polyphase filters can of course be of higher order than of order 1. The following second preferred embodiment according to the present invention described in connection with Figs. 3 and 4 shows how to create a polyphase lowpass filter with branch filters second order from a state of the art allpass filter second order.

Such state of the art allpass filter second order is shown in Fig. 4. The difference to the state of the art allpass filter first order shown in Fig. 2a is that the output signal u(k) is not the sum generated by first adder 103, but a second filter stage follows to generate this signal. Therefore, the output signal u(k) is generated as a sum signal of a further adder 106 that receives the output signal of the output delay element 102 as a first summand. The second summand of said further adder 106 is generated by multiplying the difference of the sum signal produced by the adder 103 and the delayed output signal u(k) by a multiplication factor χ with a further multiplier 109. The time delayed output signal u(k) is generated by a second output delay element 107.

The transfer function of such an allpass filter second order is shown in equation (11):

$$H_{ap.\ 2^{nd}\ order}(z) = \frac{U(z)}{T(z)} = \frac{\alpha z + 1}{z + \alpha} \cdot \frac{\chi z + 1}{z + \chi} \qquad (11)$$

Therefore, with the transfer function of a polyphase lowpass filter described in equation (1), the transfer function for the polyphase allpass branch filters with 2 coefficients follows as shown in equation (12):

$$H_r(z^N) = \frac{\beta_r z^N + 1}{z^N + \beta_r} \cdot \frac{\delta_r z^N + 1}{z^N + \delta_r} \qquad (12)$$

With equations (1) and (12) follows for the transfer function of the polyphase lowpass filter the following equation (13):

$$H_{lp}(z^N) = \sum_{r=0}^{N-1} z^{-r} \frac{\beta_r z^N + 1}{z^N + \beta_r} \cdot \frac{\delta_r z^N + 1}{z^N + \delta_r} \qquad (13)$$

For the polyphase lowpass filter with branch allpass filters of order 2 · N according to the present invention follows that all delay elements of order 1 shown in Fig. 4 have to be replaced with delay elements of order N and the sampling rate of each branch input signal is changed to $f_S' = f_S / N$ with f_S being the sampling rate of the input signal t(k).

According to the second preferred embodiment of the present invention the polyphase filter with branch filters of order 2 · N aditionally respectively comprises N time-multiplex coefficients α_r and χ_r with r = 0, 1, ..N - 1 instead of

the coefficients α and χ shown in Fig. 4. Therefore, the polyphase filter according to the second embodiment of the present invention as shown in Fig. 3 comprises aditionally to all components shown in Fig. 1: a second adder 6 that receives the output signal of the second delay element 2 at a first input for the first summand; a third delay element 7 with a delay N that receives the sum produced by said second adder 6; a second subtracter 8 that receives the sum produced by said first adder 3 at a first input for the minuend and the output signal of the third delay element 7 at a second input for the subtrahend; and a second multiplier 9 that receives the calculated difference of the second subtracter 8, multiplies it respectively with a predetermined multiplication coefficient $\chi(k)$ and outputs the calculated product to a second input of the second adder 6 that receives the second summand, wherein the sum produced by said second adder 6 builds the output signal u(k) of the branch filters.

The transfer function of the N time-multiplexed allpass filters $2N^{th}$ order included in the polyphase filter according to the second preferred embodiment are given in the following equation (15):

$$H_{ap_r',\ 2^{nd}\ order}(z) = z^{-r}\,\frac{\alpha_r z^N + 1}{z^N + \alpha_r}\cdot\frac{\chi_r z^N + 1}{z^N + \chi_r} \qquad (15)$$

with r = 0, 1, ..N - 1.

The coefficients of the N time-multiplexed allpass filters $2N^{th}$ order can be achieved by comparing equations (13) and (15). The coefficients α_r and χ_r of the N time-multiplexed allpass filters are the same as the coefficients β_r and δ_r of the polyphase lowpass filter, as it is shown in equation (16):

$$\begin{aligned} \alpha_r &= \beta_r \qquad \text{for } r = 0, 1, \ldots, N-1 \\ \chi_r &= \delta_r \qquad \text{for } r = 0, 1, \ldots, N-1 \end{aligned} \qquad (16)$$

It can be seen from both preferred embodiments according to the present invention described above that the present invention allows a very easy design of polyphase filters of order $x \cdot N$ consisting of N allpass filters of order $x \cdot N$ and having a desireable factor N. According to the present invention within the structure of an allpass filter of order x all delay elements with a delay 1 are replaced by delay elements with a delay N and so the input sampling rate of the branch filters is decreased to a sampling rate $f_S' = f_S / N$ with f_S being the sampling rate of the input signal t(k) of the polyphase filter.

Preferably every multiplier included within the allpass filter of order x comprises N time-multiplexed multiplication coefficients that are used in a predetermined order, e. g. $a(k) = a_{(k \bmod N)}$.

Further preferably everyone of said multipliers has quantized coefficients so that it can be realized by at least one shift register, at least one adder and at least one subtracter.

An IQ-generator according to the present invention is described in connection with Figs. 5 to 9.

Fig. 5 shows on the left hand side an analog bandpass signal s(t) with a center frequency f_0 which is sampled by an A/D-converter with a sampling rate f_S. The sampled bandpass signal s(k) is passed to a digital IQ-filter according to the present invention that mixes the sampled bandpass signal s(k) to a complex baseband signal, performs a sampling rate decimation with a decimation factor of N and a noise shaping which depends on the number of branch filters N of the polyphase filter. The output signal of the IQ-filter is the complex baseband signal $w(l) = w_I(l) + jw_Q(l)$ with a sampling rate of $f_S' = f_S/N$.

Fig. 6 shows the block diagram of the digital IQ-filter according to the present invention that includes a filter block 22 consisting of N time-multiplexed allpass filters according to the present invention. The incoming sampled bandpass signal s(k) gets multiplied with a signal A(k) by an multiplier 21 before the resulting signal t(k) is input to the N time multiplexed allpass filters 22 according to the present invention which outputs an output signal u(k). To generate the inphase component $w_I(l)$ of the complex baseband signal w(l) the output signal u(k) of the polyphase filter according to the present invention is subjected to a multiplication with the function $B(k) \cdot \cos(2\pi f_0/f_S \cdot k)$ in a multiplier 23 before it is supplied as a first summand to an adder 24 which receives its own output signal delayed by a delay element 26 with a delay T via a switch $S_I(k)$25 as second summand. The output signal of the adder 24 gets decimated by N in a sampling rate decimation unit 27 which outputs the inphase component $w_I(l)$ of the complex baseband signal w(l). To generate the quadrature-component $w_Q(l)$ of the complex baseband signal w(l) the output signal u(k) of the polyphase filter according to the present invention is subjected to a multiplication with the funktion $B(k) \cdot \sin(2\pi f_0/f_S \cdot k)$ in a multi-

plier 28 before it is supplied as a first summand to an adder 29 which receives its own output signal delayed by a delay element 31 with a delay T via a switch $S_Q(k)$ 30 as second summand. The output signal of the adder 29 gets decimated by N in a sampling rate decimation unit 32 which outputs the quadrature component $w_Q(l)$ of the complex baseband signal $w(l)$.

The switch $s_I(k)$25 for the inphase component of the complex baseband signal and the switch $S_Q(k)$ 30 for the quadrature component of the complex baseband signal are switched in the following way:

$$S_I(k) = S_Q(k) = \begin{cases} 0 & \text{for } k \bmod N = 0 \\ 1 & \text{else} \end{cases} \qquad (17)$$

The center frequency f_0 of the A/D-converter input signal s(t) is given by equation (18) or (19):

$$f_0 = f_s\left(\frac{n \pm 0.5}{N} + m\right) \qquad (18)$$

$$f_0 = f_s\left(\frac{n}{N} + m\right) \qquad (19)$$

with N: decimation factor

n: integer in the range of $\left[-\frac{N}{2}, \ldots, \frac{N}{2}\right]$

m: integer

A(k) and B(k) must be chosen dependent on the center frequency of the A/D-converter input signal. In case of a center frequency f_0 calculated with equation (18) A(k) and B(k) are given by equation (20):

$$A(k) = B(k) = (-1)^{\text{floor}\left(\frac{k}{N}\right)} \qquad (20)$$

In case of a center frequency f_0 calculated with equation (19) A(k) is given by equation (21):

$$A(k) = B(k) = 1 \qquad (21)$$

In the special case of the following equation (22):

$$f_0 = f_s\left(\frac{1}{4} + m\right) \tag{22}$$

with m: integer, which is also called quarter period sampling, the carrier multiplication at the output of the modified allpass filter is not necessary. In this case, the block diagram shown in Fig. 6 can be reduced to the block diagram shown in Fig. 7.

Here, the output signal u(k) of the N time multiplexed allpass filters 22 according to the present invention is fed directly as a first summand to an adder 33 which outputs the IQ-multiplexed complex baseband signal $w(l) = w_I(l) + jw_Q(l)$. The adder 33 receives the IQ-multiplexed complex baseband signal delayed by two delay elements 35, 36 each having a delay T via a switch S7 34 as second summand. The switch 34 is switched in the following way:

$$S_7 = \begin{cases} 0 & \text{for } k \bmod N = 0,1 \\ 1 & \text{else} \end{cases} \tag{23}$$

The output signal of the adder 33 gets decimated by N/2 in a sampling rate decimation unit 37 which outputs the multiplexed complex baseband signal w(l).

Depending on the required sideband for the IQ-generation, the factor A(k) is calculated by equation (24) or equation (25):

$$A(k) = (-1)^{\mathrm{floor}\left(\frac{k}{2}\right)} \tag{24}$$

$$A(k) = (-1)^{\mathrm{floor}\left(\frac{k-1}{2}\right)} \tag{25}$$

As mentioned above, the output signal of the IQ-filter described in Fig. 7 is the time-multiplexed complex baseband signal with a sampling rate of $f_S' = f_S/N$.

Figs. 8 and 9 show an example of an IQ-filter according to the present invention comprising a polyphase filter with branch filters of order 2N according to the present invention. Fig. 8 shows that the polyphase filter of order 2N as shown in Fig. 3 is used as polyphase filter 22 according to the present inven-

tion as it is shown in Fig. 7. In Fig. 8 also quarter period sampling is used so that the carrier multiplication at the output of the polyphase filter according to the present invention as shown in Fig. 6 is not necessary.

In the shown example the decimation factor N is chosen to N = 6. The coefficients of the IQ-filter are designed for a DAB-signal with a bandwidth of 1.536 MHz. The sampling frequency is chosen to 12.288 MHz and the center frequency of the input signal is chosen to f_0 = 3.072 MHz. With these values equation (22) is valid.

To decrease the hardware size, the coefficients $\alpha(k)$ and $\chi(k)$ are quantized in a way that they can be realized by shift registers, one adder and one subtracter. The following Table 1 shows the coefficients of the branch allpass filters:

r	α_r		$-\chi_r$	
5	0.21875	$2^{-2} - 2^{-5}$	0.138671875	$2^{-3} + 2^{-6} - 2^{-9}$
4	0.40625	$2^{-1} - 2^{-3} + 2^{-5}$	0.1796875	$2^{-3} + 2^{-4} - 2^{-7}$
3	0.5546875	$2^{-1} - 2^{-7} + 2^{-4}$	0.171875	$2^{-3} + 2^{-4} - 2^{-6}$
2	0.6875	$2^{-1} - 2^{-4} + 2^{-2}$	0.13671875	$2^{-3} + 2^{-6} - 2^{-8}$
1	0.8125	$1 - 2^{-2} + 2^{-4}$	0.08984375	$2^{-4} + 2^{-5} - 2^{-8}$
0	0.9375	$1 - 2^{-4}$	0.03125	2^{-5}

Table 1:

The hardware size can further be decreased when the N time multiplexed allpass filters and order are realized by a second time multiplex so that the branch allpass filters of order 2N are realized by a time multiplexed allpass filter of order N. Fig. 9 shows a block diagram of the IQ-filter realized in a time-multiplex and multiplication coefficients that are realized by shift and add operation:

The "multiplier" which is realizing the first multiplier 5 as well as the second multiplier 9 comprises a first shift register 10 having a shift value of 2^{-2} that is receiving the multiplicand and an input selector switch S2 receiving the output value of said first shift register 10 at a first fixed input terminal and the multiplicand at a second fixed input terminal, a second shift register 11, a third shift register 12 and a fourth shift register 13 each having its input connected to the moveable output terminal of said input selector switch S2, a third subtracter 14 receiving the output value of said second shift register 11 at a first input receiving the minuend, a first output selector switch S3 having its moveable input ter-

minal connected to the output of said third shift register 12, its first fixed output terminal runs free and its second fixed output terminal is connected to a second input of the third subtracter 14 receiving the subtrahend, a third adder 15 receiving the output value of said third subtracter 14 at a first input receiving the first summand and outputting the multiplied multiplicand, a second output selector switch S4 having its moveable input terminal connected to the output of said fourth register 13, its first fixed output terminal runs free and its second fixed output terminal is connected to a second input of the third adder 15 receiving the second summand.

Furtheron, to achieve the time multiplex, the incoming signal t(k) as it is shown in Fig. 6 is fed directly to a first fixed input terminal (which is marked with a 0 as all first fixed input terminals of the switches shown in the figures) of an input selector switch S0 and via a multiplicator multiplying with -1 to a second fixed terminal of this input selector switch S0. The movable terminal of the input selector switch S0 which is indicated by an arrow pointing to the first fixed terminal of the input selector switch is connected to the second fixed terminal of a first feedback selector switch S1. The movable output terminal of the first feedback selector switch S1 which is indicated by an arrow pointing to the first fixed terminal of said first feedback selector switch S1 is connected to the first delay element 1 with a delay time 6T, i. e. $2 \cdot 3 \cdot T$, that additionally comprises a latch enable input receiving the latch signal LE0 for the purpose of the time multiplex. The output of the first delay element 1 is fed via the second fixed terminal and the movable terminal of a second feedback selector switch S5 to the first input of the first adder 3. For the purpose of the time multiplex the first adder 3 is in this case an adder-subtracter and therewith the first input receives either the first summand or the minuent according to the respective function of the adder-subtracter 3. The output of the adder-subtracter 3 is fed to a first part 2a of the second delay element that has a delay T which provides the output signal u(k) of the polyphase filter 22 according to the present invention at its output. This output signal is fed to the first fixed input terminal of the first input selector switch S1 and also to a second part 2b of the second delay element having a delay 11T. The output of this delay element 2b is supplied to the first fixed terminal of the second feedback selector switch S5 and as subtrahent to the first subtracter 4 which receives the output signal of the first feedback selector switch S1 as minuent. The difference calculated by the first subtracter 4 gets multiplied with a respective coefficient $\alpha(k)$ or $\chi(k)$ as described above before it is supplied as second summand or as subtrahent to the adder-subtracter 3.

As mentioned above, the effient IQ-filter realization shown in Fig. 9 has its sampling rate decimation factor of N = 6 and the N allpass filters 2Nth order are realized time-multiplexed. Therefore, one complex output sample has to be processed in 12 output clock cycles, i. e. $f_C = 2f_S = 2 \cdot 6 \cdot f_S'$. The signal A(k) is periodic in 2 output clock samples. Therefore, the states of the IQ-filter are periodic in 24 clock cycles f_C. Table 2 below describes for every of the 24 different internal states of the IQ-filter the states of the switches that allabled with S0, S1, S2, S3, S4, S5, and S6 in the figures, the latch enable signal LE0 which is active high and the shift values of the shift registers SH0, SH1, and SH2. States that are not relevant and therefore don't care are marked by dc. Output signals w that are not defined are marked by nd.

State	S0		S1	S2	S3	S4	S5	S6	SH0	SH1	SH2	LE0	A0	W
0	0	0	1	1	1	0	1	1	0	2	dc	1	+	Q(l - 1)
1	dc		0	0	0	0	0	0	3	dc	dc	0	-	nd
2	0	1	1	1	1	1	1	0	0	0	2	1	+	nd
3	dc		0	0	1	1	0	0	2	4	1	0	-	nd
4	1	1	1	1	1	1	1	0	1	2	0	1	+	nd
5	dc		0	0	1	1	0	0	1	4	2	0	-	nd
6	1	0	1	1	1	1	1	1	1	5	2	1	+	nd
7	dc		0	0	1	1	0	0	1	2	0	0	-	nd
8	0	0	1	1	1	1	1	1	1	1	3	1	+	nd
9	dc		0	0	1	1	0	0	1	3	0	0	-	nd
10	0	1	1	1	1	0	1	1	2	3	dc	1	+	I(l)
11	dc		0	0	1	1	0	0	1	5	2	0	-	nd
12	1	1	1	1	1	0	1	1	0	2	dc	1	+	Q(l)
13	dc		0	0	0	0	0	0	3	dc	dc	0	-	nd
14	1	0	1	1	1	1	1	0	0	0	2	1	+	nd
15	dc		0	0	1	1	0	0	2	4	1	0	-	nd
16	0	0	1	1	1	1	1	0	1	2	0	1	+	nd
17	dc		0	0	1	1	0	0	1	4	2	0	-	nd
18	0	1	1	1	1	1	1	1	1	5	2	1	+	nd
19	dc		0	0	1	1	0	0	1	2	0	0	-	nd
20	1	1	1	1	1	1	1	1	1	1	3	1	+	nd
21	dc		0	0	1	1	0	0	1	3	0	0	-	nd
22	1	0	1	1	1	0	1	1	2	3	dc	1	+	I(l + 1)
23	dc		0	0	1	1	0	0	1	5	2	0	-	nd

Table 2:

Depending on the sideband that is required for the IQ-generation, the switch S0 is switched according to the left or right states that are described in the column of S0 in Table 2.

Preferably the filter can be used in a combined DAB/FM/AM-receiver and in case of DAB-reception, the input signal with a center frequency of

f_0 = 3.072 MHz is sampled with a sampling rate of f_S = 12.288 MHz, in case of FM-reception, the input signal with a center frequency of f_0 = 10.75 MHz is sampled with a sampling rate of f_S = 6.144 MHz and in the case of AM-reception, the input signal with a center frequency of f_0 = 455 KHz is sampled with a sampling rate of f_S = 2.048 MHz.

A digital IQ-filter according to the present invention has a linear phase response in the passband and high suppression of mirrored frequencies, since frequency modulated signals are sensitive against group delay distorsions which are caused by filters with non-linear phase in the passband.

As can be seen, the realization of the IQ filter according to the present invention is highly efficient, since only five adders and no multipliers are required. Therefore, the digital generation of a complex baseband signal in combination with noise shaping and neighbour channel suppression with a polyphase filter according to the present invention has low realization costs.

Claims

1. Polyphase filter consisting of N branch allpass filters of order x · N to filter an input signal t(k), **characterized by**

- a structure of an allpass filter of order x comprising delay elements with a delay 1 and at least one multiplier, wherein all delay elements with a delay 1 are replaced by delay elements with a delay N, and
- a sampling rate $f_S' = f_S/N$, with f_S being the sampling rate of the input signal (t(k)).

2. Filter according to claim 1, **characterized in** that said at least one multiplier respectively comprises N time-multiplexed multiplication coefficients ($\alpha_0, \ldots, \alpha_{N-1}$; $\chi_0, \ldots, \chi_{N-1}$) that are used in a predetermined order ($\alpha(k) = \alpha_{(k \bmod N)}$; $\chi(k) = \chi_{(k \bmod N)}$).

3. Filter according to claim 1 or 2, **characterized by**:

- a first delay element (1) with a delay N that receives the input signal (t(k));
- a first adder (3) that receives the output signal of said first delay element (1) at a first input for the first summand;
- a second delay element (2) with a delay N that receives the sum produced by said first adder (3);
- a first subtracter (4) that receives the input signal (t(k)) at a first input for the minuend and the output signal of the second delay element (2) at a second input for the subtrahend; and
- a first multiplier (5) that receives the calculated difference of the first subtracter (4), multiplies it respectively with a predetermined multiplication coefficient (α(k)) and outputs the calculated product to a second input of the first adder (3) that receives the second summand, wherein
- in case x equals to 1 the sum produced by said first adder (3) builds the output signal (u(k)) of the branch allpass filters.

4. Filter according to claim 3, **characterized by**:

- a second adder (6) that receives the output signal of the second delay element (2) at a first input for the first summand;

- a third delay element (7) with a delay N that receives the sum produced by said second adder (6);

- a second subtracter (8) that receives the sum produced by said first adder (3) at a first input for the minuend and the output signal of the third delay element (7) at a second input for the subtrahend; and

- a second multiplier (9) that receives the calculated difference of the second subtracter (8), multiplies it respectively with a predetermined multiplication coefficient ($\chi(k)$) and outputs the calculated product to a second input of the second adder (6) that receives the second summand, wherein

- in case x equals to 2 the sum produced by said second adder (6) builds the output signal (u(k)) of the branch allpass filters.

5. Filter according to anyone of claims 2 to 4, **characterized in** that every one of said at least one multipliers (5, 9) has quantised coefficients so that it can be realised by at least one shift register, at least one adder or at least one subtracter.

6. Filter according to claim 5, **characterized in** that one multiplier (5, 9) comprises:

- a first shift register (10) having a shift value of 2^{-2} that is receiving the multiplicand and,

- an input selector switch (S2) receiving the output value of said first shift register (10) at a first fixed input terminal and the multiplicand at a second fixed input terminal,

- a second shift register (11), a third shift register (12) and a fourth shift register (13) each having its input connected to the moveable output terminal of said input selector switch (S2),

- a third subtracter (14) receiving the output value of said second shift register (11) at a first input receiving the minuend,

- a first output selector switch (S3) having its moveable input terminal connected to the output of said third shift register (12), its first fixed output terminal runs free and its second fixed output terminal is connected to a second input of the third subtracter (14) receiving the subtrahend,

- a third adder (15) receiving the output value of said third subtracter (14) at a first input receiving the first summand and outputting the multiplied multiplicand,

- a second output selector switch (S4) having its moveable input terminal connected to the output of said fourth shift register (13), its first fixed output terminal runs free and its second fixed output terminal is connected to a second input of the third adder (15) receiving the second summand.

7. Filter according to anyone of the preceding claims, **characterized in that** a polyphase filter of order $x \cdot N$ with $x = a$ is realised in a time multiplex and works with a clock frequency $f_C = a \cdot f_S$.

8. IQ-generator, **characterized in that** an incoming sampled bandpass signal s(k) gets multiplied by a signal $A(k)=(-1)^{floor\ (k/N)}$ before being supplied as input signal t(k) to a polyphase filter consisting of N branch allpass filters (22) of order $x \cdot N$.

9. IQ-generator according to claim 8, **characterized in that** the output signal of the polyphase branch allpass filters (22) gets multiplied by a signal $B(k) \cdot \cos(2\pi f_0/f_S \cdot k)$ to calculate the I-component of the complex baseband signal and by a signal $B(k) \cdot \sin(2\pi f_0/f_S \cdot k)$ to calculate the Q-component of the complex baseband signal with $A(k)=B(k)=(-1)^{floor(k/n)}$.

10. IQ-generator according to claim 8 or 9, **characterized by** one polyphase filter according to anyone of claims 1 to 7 to filter the I-component and the Q-component of a complex baseband signal.

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MÜLLER & HOFFMANN

Sony International (Europe) GmbH File: 50.679

24.05.2000

Abstract

A Digital Filter For IQ-Generation, Noise Shaping and Neighbour Channel Suppression

A polyphase filter of order $x \cdot N$ that is building N allpass filters of order $x \cdot N$ according to the present invention has a structure of an allpass filter of order x comprising delay elements with a delay 1 and at least one multiplier, wherein all delay elements with a delay of 1 are replaced by delay elements with a delay of N and the sampling rate of $f_S' = f_S/N$ with f_S being the sampling rate of the input signal.

Preferably the multiplier included in the structure of the allpass filter of order x comprises N-time multiplex multiplication coefficients that are used in a predetermined order.

(Fig. 1)

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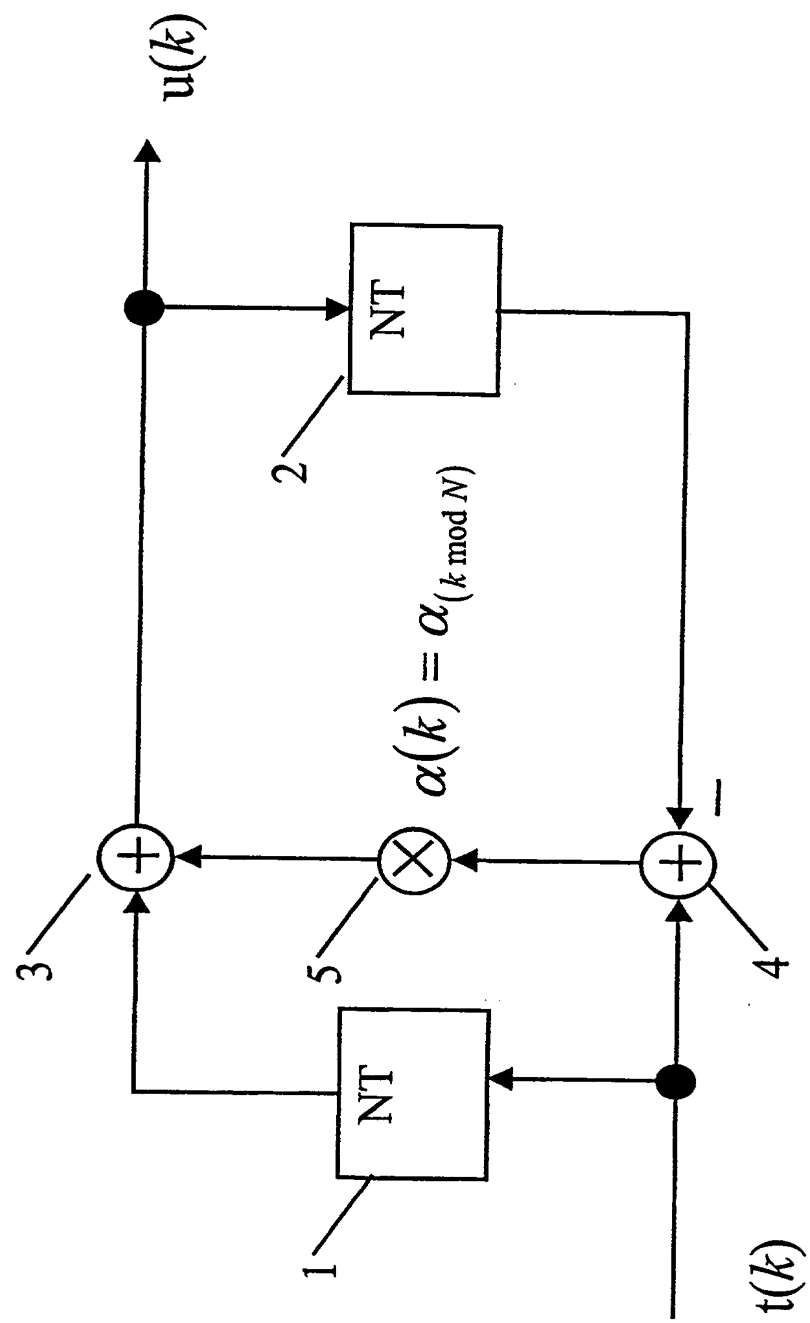


Figure 1

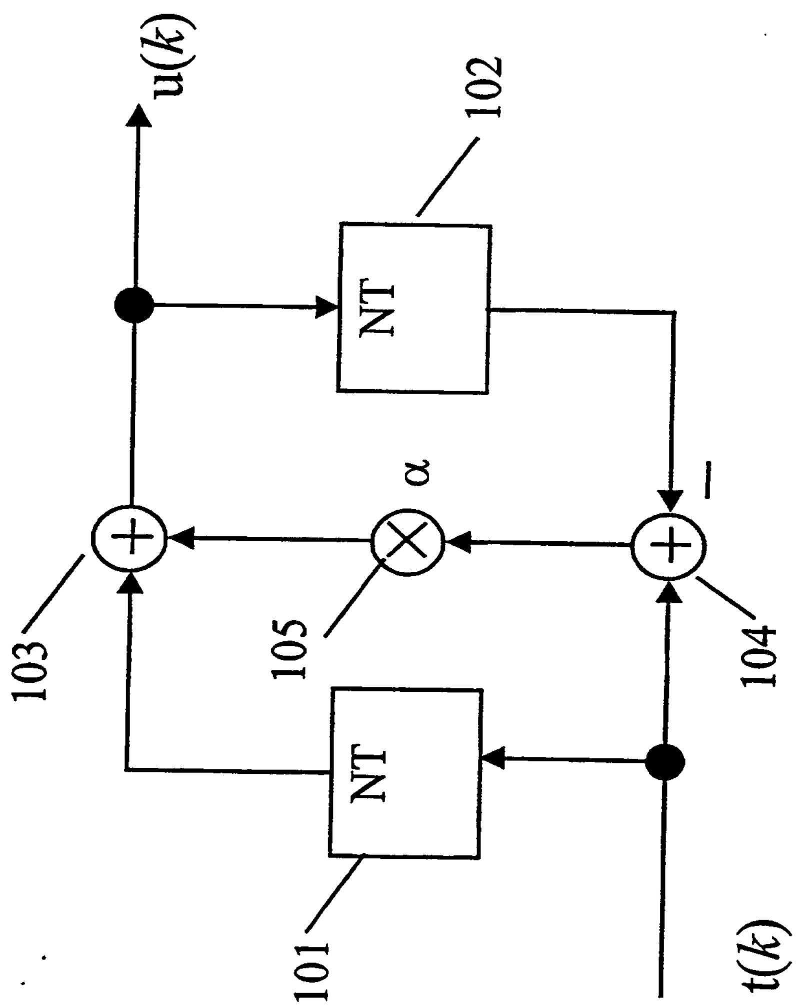


Figure 2a

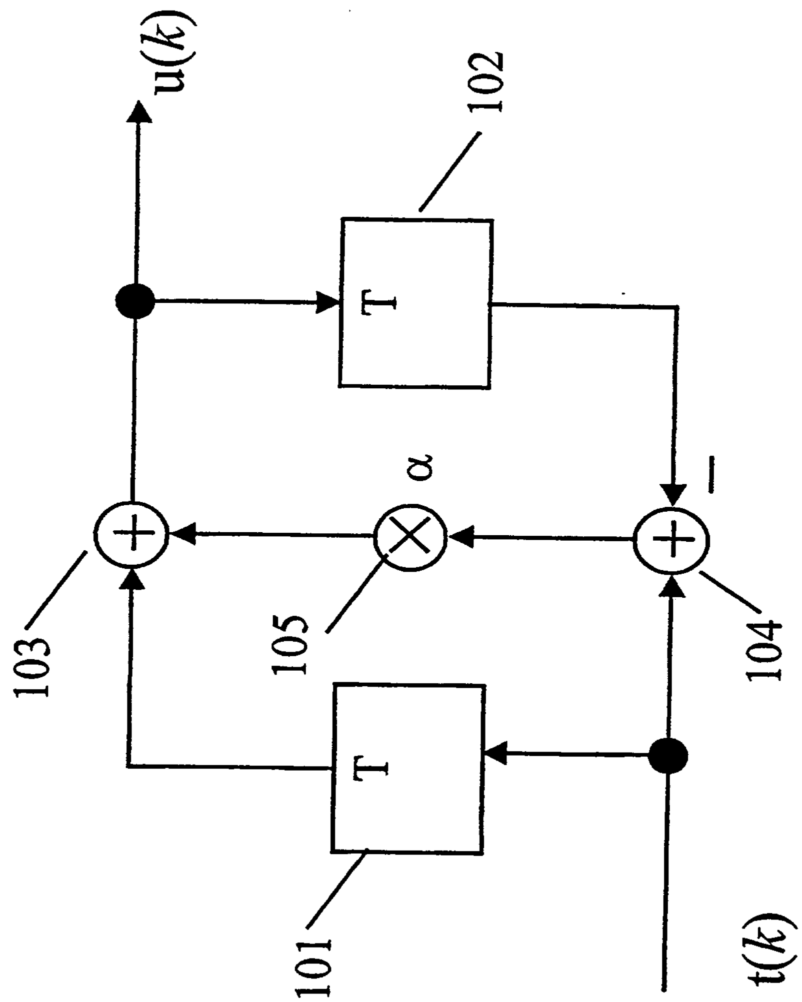


Figure 2b

Figure 3

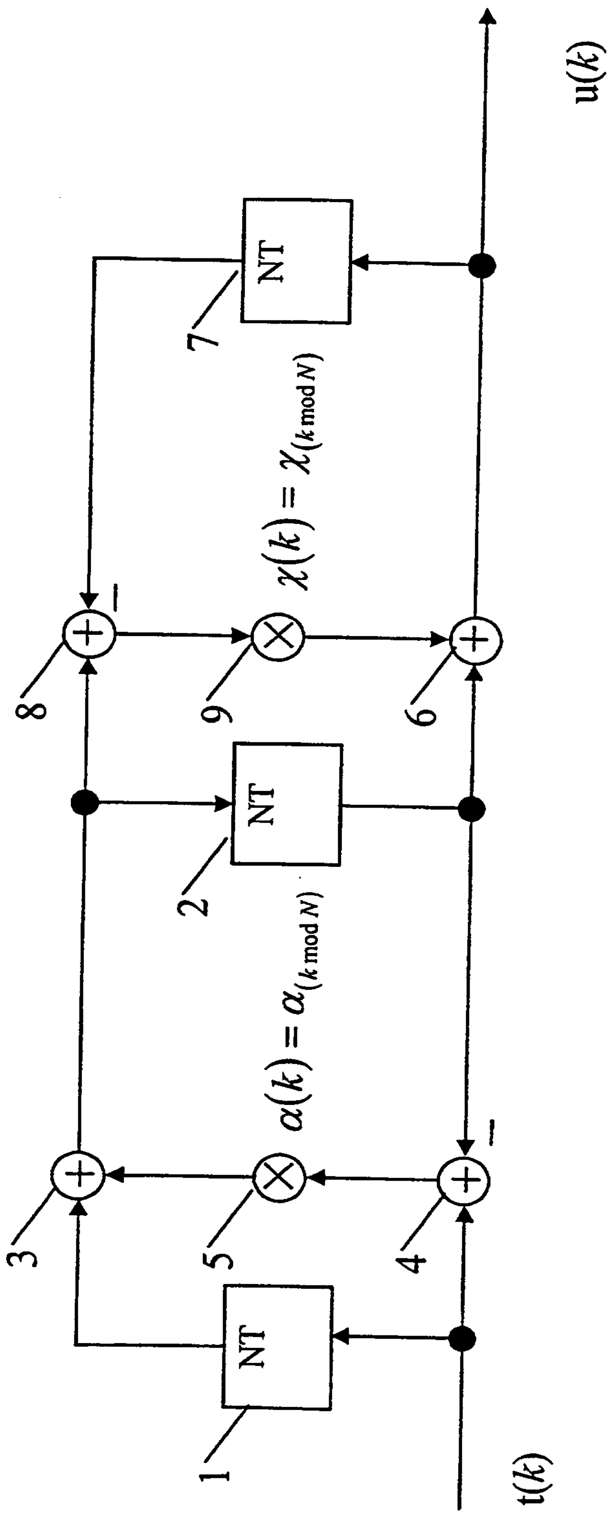


Figure 4

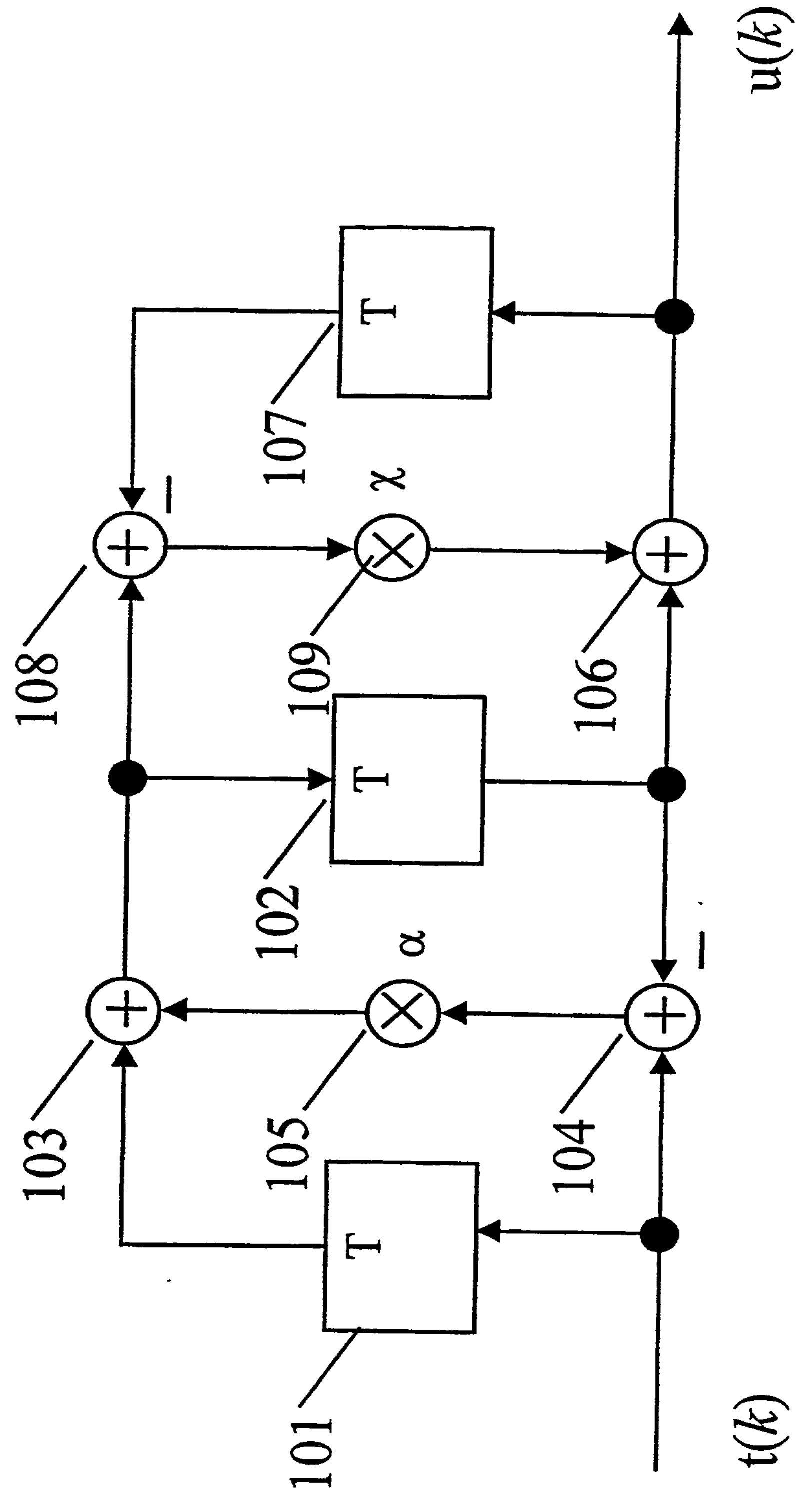
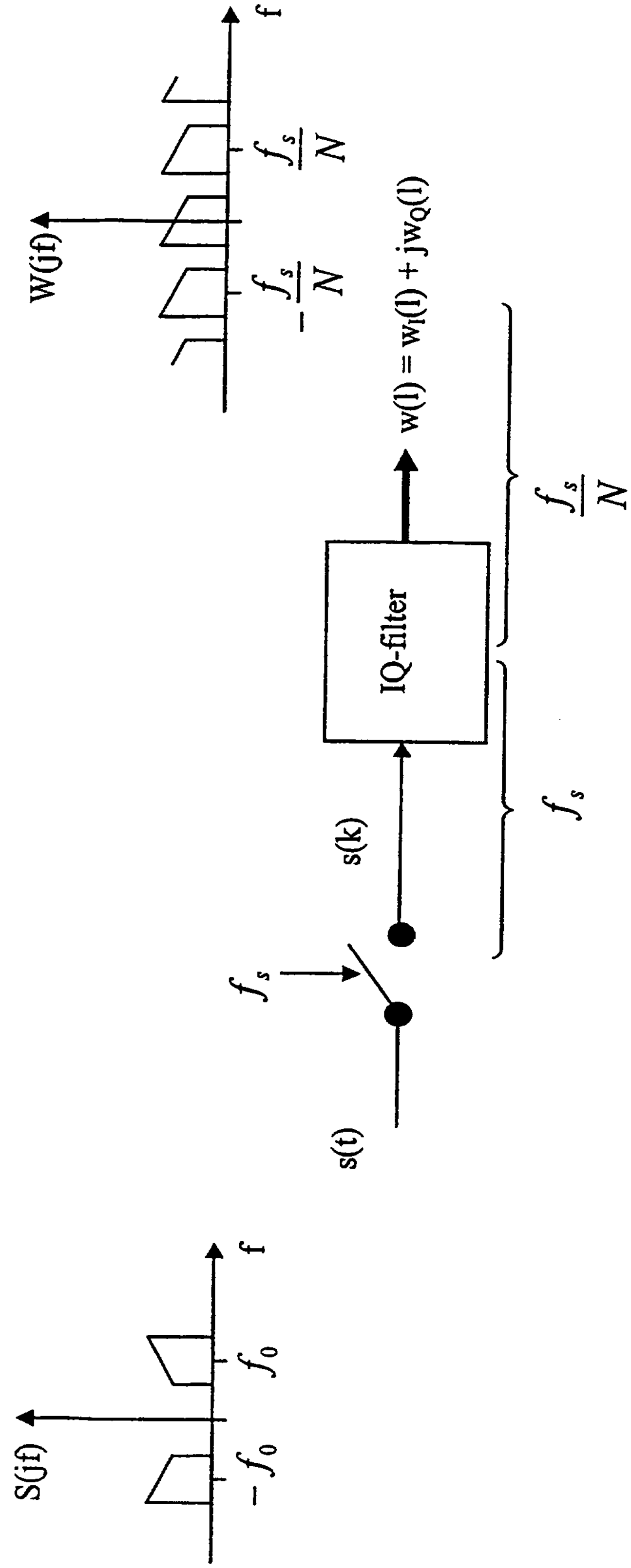


Figure 5



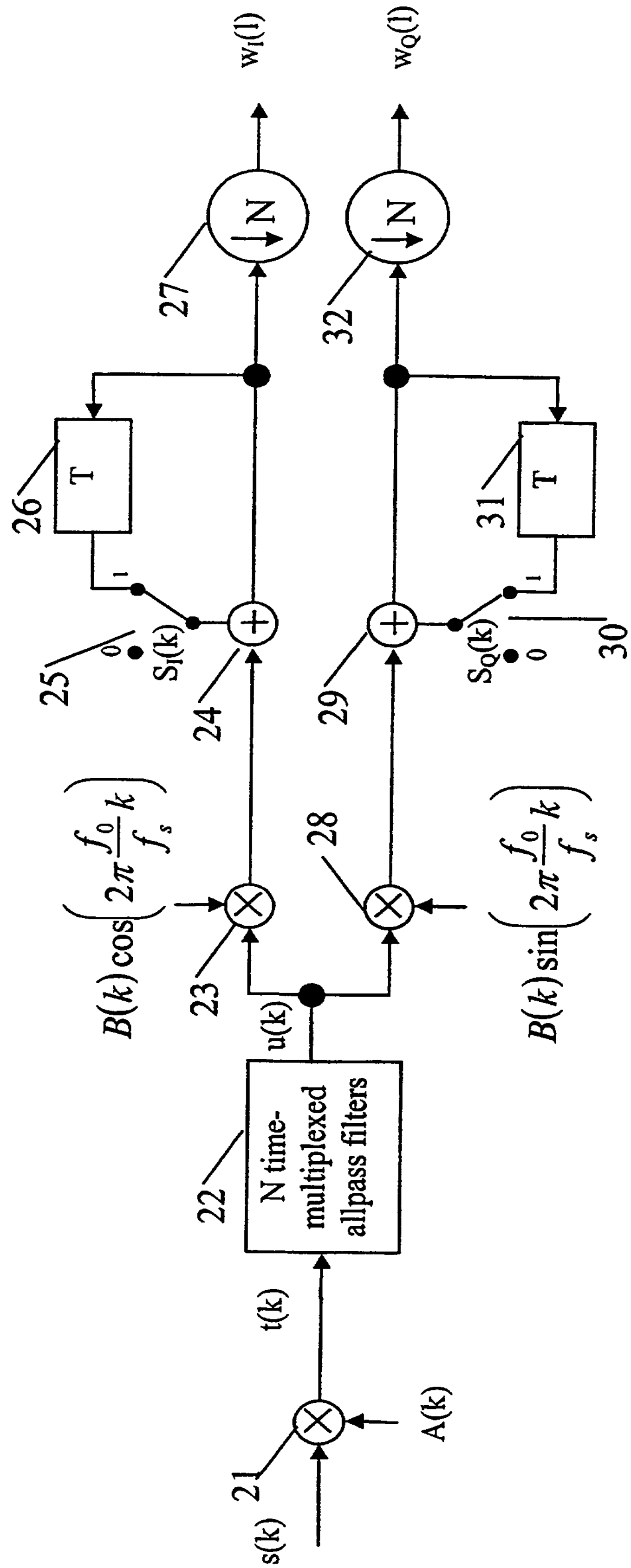

s(k)
21
A(k)
t(k)
22
N time-multiplexed allpass filters
u(k)
23
$B(k)\cos\left(2\pi\frac{f_0}{f_s}k\right)$
28
$B(k)\sin\left(2\pi\frac{f_0}{f_s}k\right)$
24
29
25
$S_I(k)$
$S_Q(k)$
0
1
30
26
31
T
T
27
32
N
N
$w_I(l)$
$w_Q(l)$

Figure 6

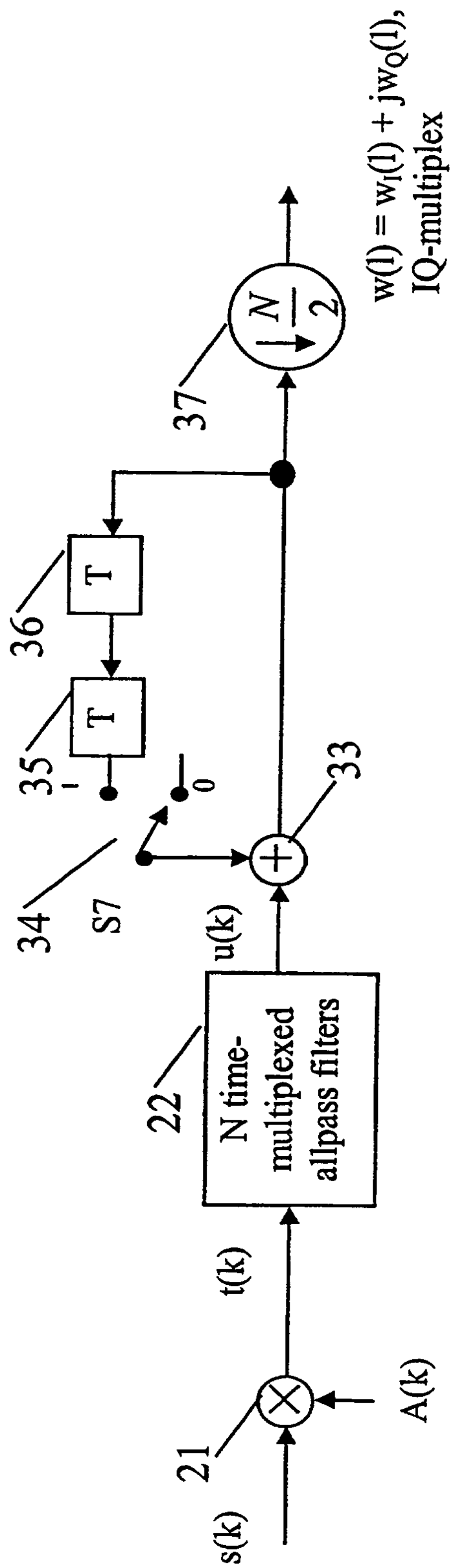

s(k)
21
A(k)
t(k)
22
N time-multiplexed allpass filters
u(k)
S7
34
1
0
35
T
36
T
33
37
$\downarrow \frac{N}{2}$
$w(l) = w_I(l) + jw_Q(l)$,
IQ-multiplex

Figure 7

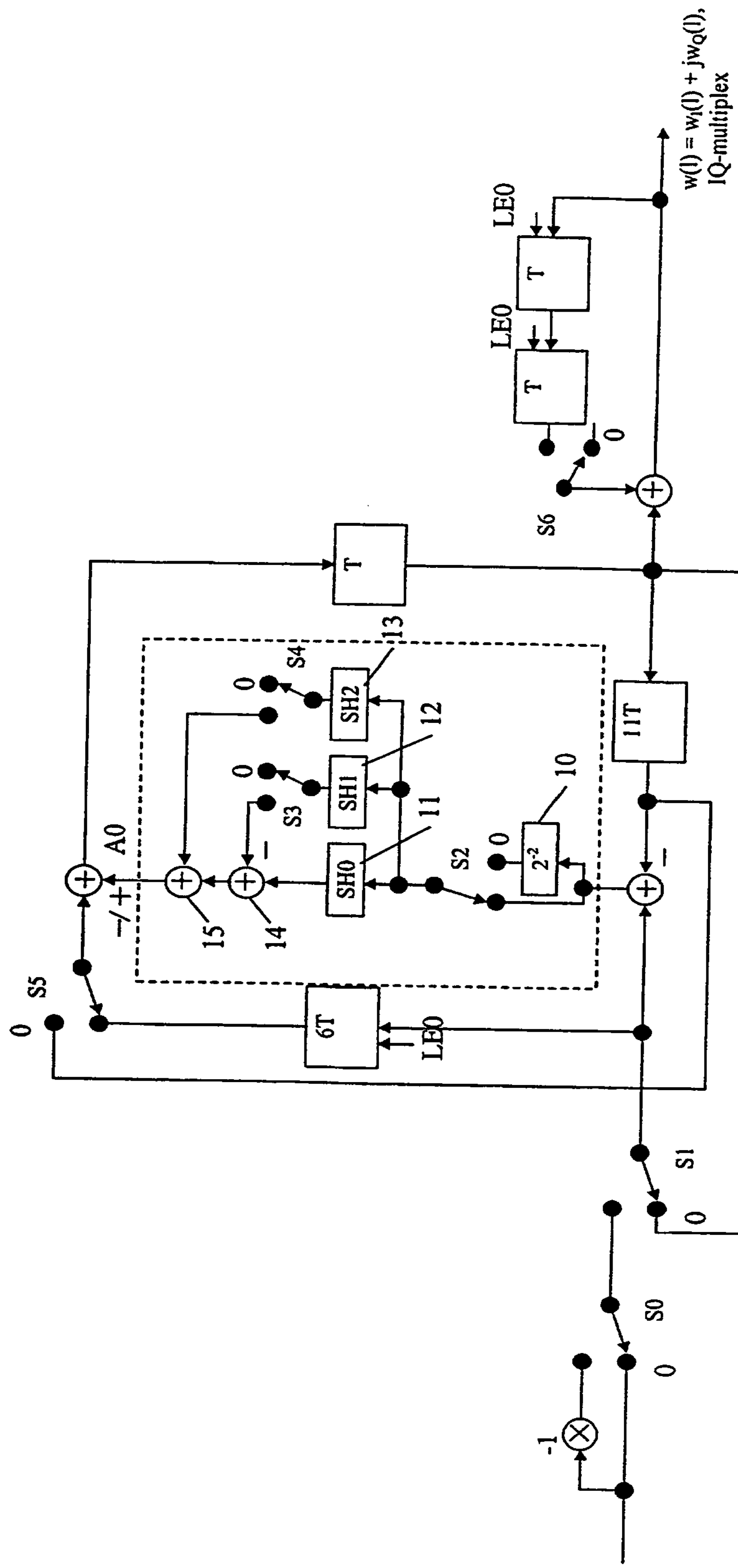
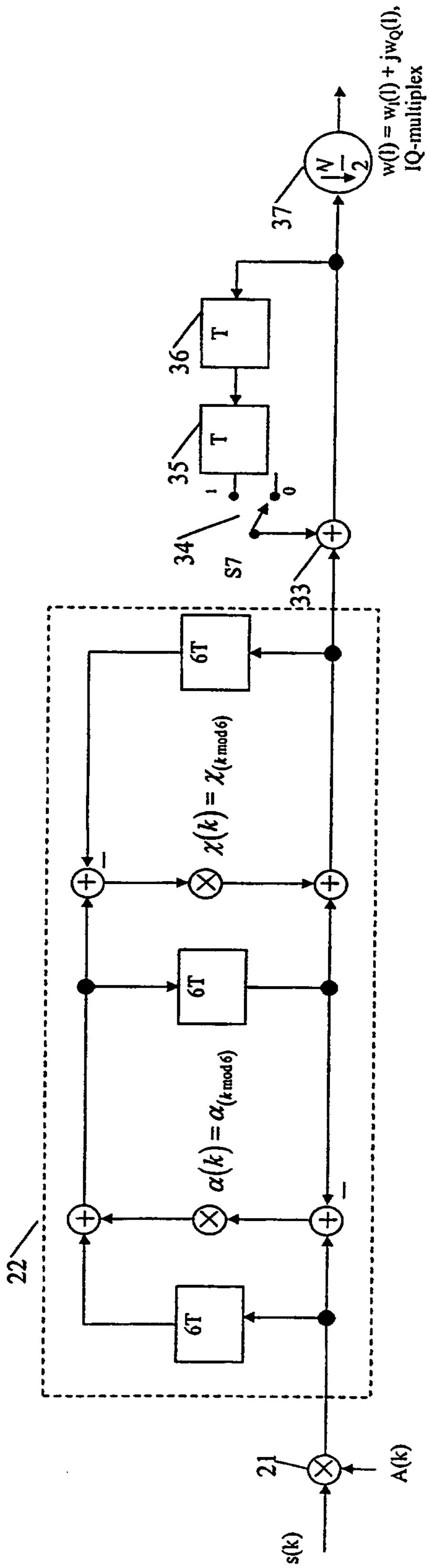

w(l) = w_I(l) + jw_Q(l),
IQ-multiplex
LE0
LE0
T
T
0
S6
T
S4
SH2
SH1
SH0
S3
S2
2^-2
11T
A0
S5
6T
LE0
S1
S0
0
-1
10
11
12
13
14
15

Figure 9

Figure 8


s(k)
A(k)
21
22
6T
6T
6T
$\alpha(k) = \alpha_{(k \bmod 6)}$
$\chi(k) = \chi_{(k \bmod 6)}$
33
34
S7
1
0
35
36
T
T
37
$\frac{N}{2}$
$w(l) = w_I(l) + jw_Q(l)$,
IQ-multiplex